

NLAS5223B, NLAS5223BL

Ultra-Low 0.35 Ω Dual SPDT Analog Switch

The NLAS5223B is an advanced CMOS analog switch fabricated in Sub-micron silicon gate CMOS technology. The device is a dual Independent Single Pole Double Throw (SPDT) switch featuring Ultra-Low R_{ON} of 0.35 Ω , at $V_{CC} = 4.3$ V.

The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver.

Features

- Ultra-Low R_{ON} , 0.35 Ω (typ) at $V_{CC} = 4.3$ V
- NLAS5223B Interfaces with 2.8 V Chipset
- NLAS5223BL Interfaces with 1.8 V Chipset
- Single Supply Operation from 1.65–4.5 V
- Full 0– V_{CC} Signal Handling Capability
- High Off-Channel Isolation
- Low Standby Current, < 50 nA
- Low Distortion
- R_{ON} Flatness of 0.15 Ω
- High Continuous Current Capability
± 300 mA Through Each Switch
- Large Current Clamping Diodes at Analog Inputs
± 300 mA Continuous Current Capability
- Package:
 - ◆ 1.4 x 1.8 x 0.75 mm WQFN10 Pb-Free
 - ◆ 1.4 x 1.8 x 0.55 mm UQFN10 Pb-Free
- These are Pb-Free Devices

Applications

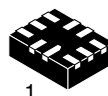
- Cell Phone Audio Block
- Speaker and Earphone Switching
- Ring-Tone Chip / Amplifier Switching
- Modems



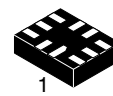
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



**WQFN10
CASE 488AQ**

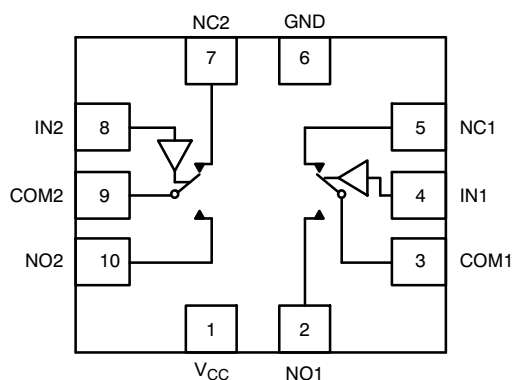


**UQFN10
CASE 488AT**



XX = Specific Device Code
 AD = NLAS5223BMNR2G
 AE = NLAS5223BLMNR2G
 AP = NLAS5223BMUR2G
 M = Date Code/Assembly Location
 ■ = Pb-Free Device

(Note: Microdot may be in either location)



FUNCTION TABLE

| IN 1, 2 | NO 1, 2 | NC 1, 2 |
|---------|---------|---------|
| 0 | OFF | ON |
| 1 | ON | OFF |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NLAS5223B, NLAS5223BL

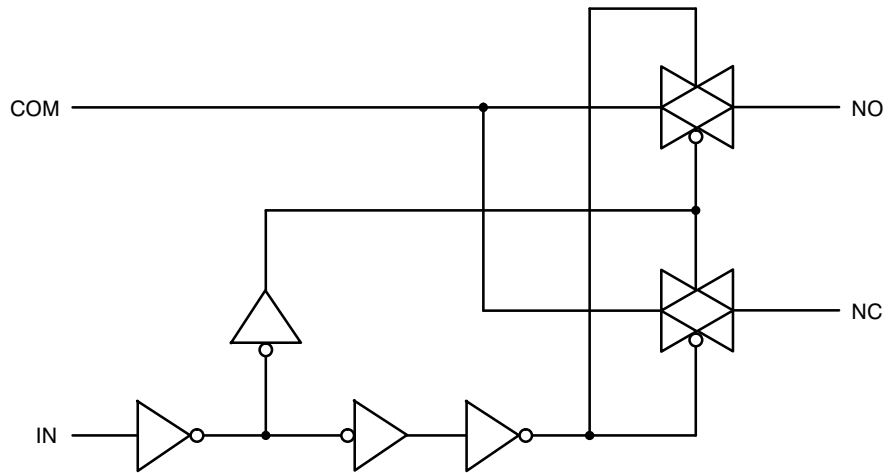


Figure 1. Logic Equivalent Circuit

PIN DESCRIPTION

| QFN PIN # | Symbol | Name and Function |
|-------------|------------------------|-------------------------|
| 2, 5, 7, 10 | NC1 to NC2, NO1 to NO2 | Independent Channels |
| 4, 8 | IN1 and IN2 | Controls |
| 3, 9 | COM1 and COM2 | Common Channels |
| 6 | GND | Ground (V) |
| 1 | V _{CC} | Positive Supply Voltage |

NLAS5223B, NLAS5223BL

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|--|--------------------------------------|------|
| V_{CC} | Positive DC Supply Voltage | -0.5 to +5.5 | V |
| V_{IS} | Analog Input Voltage (V_{NO} , V_{NC} , or V_{COM}) | $-0.5 \leq V_{IS} \leq V_{CC} + 0.5$ | V |
| V_{IN} | Digital Select Input Voltage | $-0.5 \leq V_{IN} \leq +5.5$ | V |
| I_{anI1} | Continuous DC Current from COM to NC/NO | ± 300 | mA |
| $I_{anI-pk1}$ | Peak Current from COM to NC/NO, 10 Duty Cycle (Note 1) | ± 500 | mA |
| I_{clmp} | Continuous DC Current into COM/NO/NC with Respect to V_{CC} or GND | ± 100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Defined as 10% ON, 90% OFF Duty Cycle.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------|--|------|--|------|
| V_{CC} | DC Supply Voltage | 1.65 | 4.5 | V |
| V_{IN} | Digital Select Input Voltage (OVT) Overvoltage Tolerance | GND | 4.5 | V |
| V_{IS} | Analog Input Voltage (NC, NO, COM) | GND | V_{CC} | V |
| T_A | Operating Temperature Range | -40 | +85 | °C |
| t_r, t_f | Input Rise or Fall Time, SELECT | | 20 10 | ns/V |
| | | | $V_{CC} = 1.6\text{ V} - 2.7\text{ V}$ $V_{CC} = 3.0\text{ V} - 4.5\text{ V}$ | |

NLAS5223B, NLAS5223BL

NLAS5223B DC CHARACTERISTICS – DIGITAL SECTION (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Limit | | Unit |
|------------------|---|---|-----------------|------------------|----------------|------|
| | | | | 25°C | -40°C to +85°C | |
| V _{IH} | Minimum High-Level Input Voltage, Select Inputs | | 3.0 | 1.4 | 1.4 | V |
| | | | 4.3 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage, Select Inputs | | 3.0 | 0.7 | 0.7 | V |
| | | | 4.3 | 0.8 | 0.8 | |
| I _{IN} | Maximum Input Leakage Current, Select Inputs | V _{IN} = V _{CC} or GND | 4.3 | ±0.1 | ±1.0 | µA |
| I _{OFF} | Power Off Leakage Current | V _{IN} = V _{CC} or GND | 0 | ±0.5 | ±2.0 | µA |
| I _{CC} | Maximum Quiescent Supply Current (Note 2) | Select and V _{IS} = V _{CC} or GND | 1.65 to 4.5 | ±1.0 | ±2.0 | µA |

2. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

NLAS5223B DC ELECTRICAL CHARACTERISTICS – ANALOG SECTION

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Maximum Limit | | | | Unit |
|--|--|--|-----------------|--------------------------|------|----------------|------|------|
| | | | | 25°C | | -40°C to +85°C | | |
| | | | | Min | Max | Min | Max | |
| R _{ON} | NC/NO On-Resistance (Note 3) | V _{IN} = V _{IL} or V _{IN} = V _{IH} V _{IS} = GND to V _{CC} I _{COM} = 100 mA | 3.0 | | 0.4 | | 0.5 | Ω |
| | | | 4.3 | | 0.35 | | 0.4 | |
| R _{FLAT} | NC/NO On-Resistance Flatness (Notes 3 and 4) | I _{COM} = 100 mA V _{IS} = 0 to V _{CC} | 3.0 | | 0.16 | | 0.20 | Ω |
| 4.3 | | 0.11 | | 0.14 | | | | |
| ΔR _{ON} | On-Resistance Match Between Channels (Notes 3 and 5) | V _{IS} = 1.5 V; I _{COM} = 100 mA V _{IS} = 2.2 V; I _{COM} = 100 mA | 3.0 | | 0.05 | | 0.05 | Ω |
| | | | 4.3 | | 0.05 | | 0.05 | |
| I _{NC(OFF)} I _{NO(OFF)} | NC or NO Off Leakage Current (Note 3) | V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 0.3 V V _{COM} = 4.0 V | 4.3 | -5.0 | 5.0 | -50 | 50 | nA |
| I _{COM(ON)} | COM ON Leakage Current (Note 3) | V _{IN} = V _{IL} or V _{IH} V _{NO} 0.3 V or 4.0 V with V _{NC} floating or V _{NC} 0.3 V or 4.0 V with V _{NO} floating V _{COM} = 0.3 V or 4.0 V | 4.3 | -10 | 10 | -100 | 100 | nA |

3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

4. Flatness is defined as the difference between the maximum and minimum value of On-resistance as measured over the specified analog signal ranges.

5. ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)} between NC1 and NC2 or between NO1 and NO2.

NLAS5223B, NLAS5223BL

NLAS5223BL DC CHARACTERISTICS – DIGITAL SECTION (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Limit | | Unit |
|------------------|---|---|-----------------|------------------|----------------|------|
| | | | | 25°C | -40°C to +85°C | |
| V _{IH} | Minimum High-Level Input Voltage, Select Inputs | | 3.0 | 1.3 | 1.3 | V |
| | | | 4.3 | 1.6 | 1.6 | |
| V _{IL} | Maximum Low-Level Input Voltage, Select Inputs | | 3.0 | 0.5 | 0.5 | V |
| | | | 4.3 | 0.6 | 0.6 | |
| I _{IN} | Maximum Input Leakage Current, Select Inputs | V _{IN} = 4.5 V or GND | 4.3 | ±0.1 | ±1.0 | µA |
| I _{OFF} | Power Off Leakage Current | V _{IN} = 4.5 V or GND | 0 | ±0.5 | ±2.0 | µA |
| I _{CC} | Maximum Quiescent Supply Current (Note 6) | Select and V _{IS} = V _{CC} or GND | 1.65 to 4.5 | ±1.0 | ±2.0 | µA |

6. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

NLAS5223BL DC ELECTRICAL CHARACTERISTICS – ANALOG SECTION

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Maximum Limit | | | | Unit |
|--|--|--|-----------------|--------------------------|------|----------------|------|------|
| | | | | 25°C | | -40°C to +85°C | | |
| | | | | Min | Max | Min | Max | |
| R _{ON} | NC/NO On-Resistance (Note 7) | V _{IN} = V _{IL} or V _{IN} = V _{IH} V _{IS} = GND to V _{CC} I _{COM} = 100 mA | 3.0 | | 0.4 | | 0.5 | Ω |
| | | | 4.3 | | 0.35 | | 0.4 | |
| R _{FLAT} | NC/NO On-Resistance Flatness (Notes 7 and 8) | I _{COM} = 100 mA V _{IS} = 0 to V _{CC} | 3.0 | | 0.16 | | 0.20 | Ω |
| 4.3 | | 0.11 | | 0.14 | | | | |
| ΔR _{ON} | On-Resistance Match Between Channels (Notes 7 and 9) | V _{IS} = 1.5 V; I _{COM} = 100 mA V _{IS} = 2.2 V; I _{COM} = 100 mA | 3.0 | | 0.05 | | 0.05 | Ω |
| | | | 4.3 | | 0.05 | | 0.05 | |
| I _{NC(OFF)} I _{NO(OFF)} | NC or NO Off Leakage Current (Note 7) | V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 0.3 V V _{COM} = 4.0 V | 4.3 | -10 | 10 | -100 | 100 | nA |
| I _{COM(ON)} | COM ON Leakage Current (Note 7) | V _{IN} = V _{IL} or V _{IH} V _{NO} 0.3 V or 4.0 V with V _{NC} floating or V _{NC} 0.3 V or 4.0 V with V _{NO} floating V _{COM} = 0.3 V or 4.0 V | 4.3 | -10 | 10 | -100 | 100 | nA |

7. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

8. Flatness is defined as the difference between the maximum and minimum value of On-resistance as measured over the specified analog signal ranges.

9. ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)} between NC1 and NC2 or between NO1 and NO2.

NLAS5223B, NLAS5223BL

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | V_{CC} (V) | V_{IS} (V) | Guaranteed Maximum Limit | | | | | Unit |
|-----------|--------------------------------|---|-----------------|-----------------|--------------------------|------|-----|----------------|-----|------|
| | | | | | 25°C | | | -40°C to +85°C | | |
| | | | | | Min | Typ* | Max | Min | Max | |
| t_{ON} | Turn-On Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 3 and 4) | 2.3 - 4.5 | 1.5 | | | 50 | | 60 | ns |
| t_{OFF} | Turn-Off Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 3 and 4) | 2.3 - 4.5 | 1.5 | | | 30 | | 40 | ns |
| t_{BBM} | Minimum Break-Before-Make Time | $V_{IS} = 3.0$ $R_L = 50 \Omega$, $C_L = 35$ pF (Figure 2) | 3.0 | 1.5 | 2 | 15 | | | | ns |

| | | Typical @ 25, $V_{CC} = 3.6$ V | |
|-------------|---|--------------------------------|--|
| C_{IN} | Control Pin Input Capacitance | 3.5 | |
| $C_{NO/NC}$ | NO, NC Port Capacitance | 60 | |
| C_{COM} | COM Port Capacitance When Switch is Enabled | 200 | |

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter | Condition | V_{CC} (V) | 25°C | Unit |
|-----------|--|---|-----------------|---------|------|
| | | | | Typical | |
| BW | Maximum On-Channel -3 dB Bandwidth or Minimum Frequency Response | V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 - 4.5 | 19 | MHz |
| V_{ONL} | Maximum Feed-through On Loss | $V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 - 4.5 | -0.06 | dB |
| V_{ISO} | Off-Channel Isolation | $f = 100$ kHz; $V_{IS} = 1$ V RMS; $C_L = 5.0$ pF V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 - 4.5 | -68 | dB |
| Q | Charge Injection Select Input to Common I/O | $V_{IN} = V_{CC}$ to GND, $R_{IS} = 0 \Omega$, $C_L = 1.0$ nF $Q = C_L \times DV_{OUT}$ (Figure 6) | 1.65 - 4.5 | 38 | pC |
| THD | Total Harmonic Distortion THD + Noise | $F_{IS} = 20$ Hz to 20 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 2.0$ V RMS | 3.0 | 0.08 | % |
| VCT | Channel-to-Channel Crosstalk | $f = 100$ kHz; $V_{IS} = 1.0$ V RMS, $C_L = 5.0$ pF, $R_L = 50 \Omega$ V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 - 4.5 | -70 | dB |

10. Off-Channel Isolation = $20 \log_{10} (V_{COM}/V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

NLAS5223B, NLAS5223BL

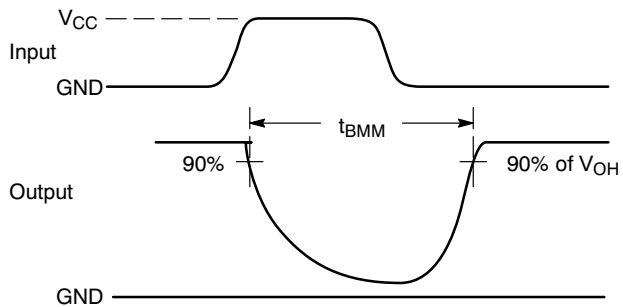
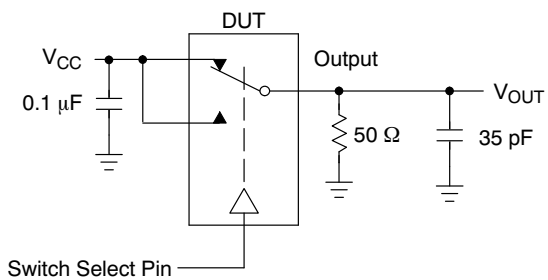


Figure 2. t_{BMM} (Time Break-Before-Make)

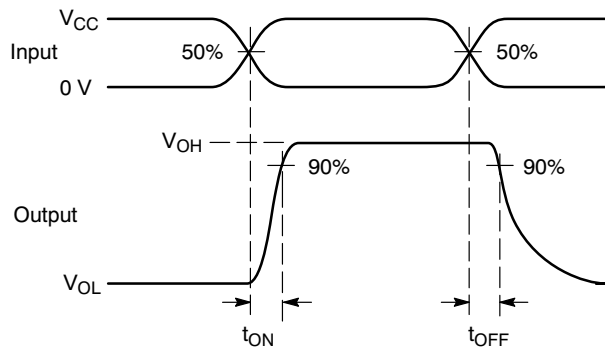
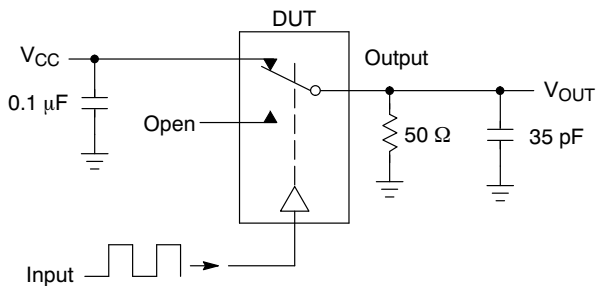


Figure 3. t_{ON}/t_{OFF}

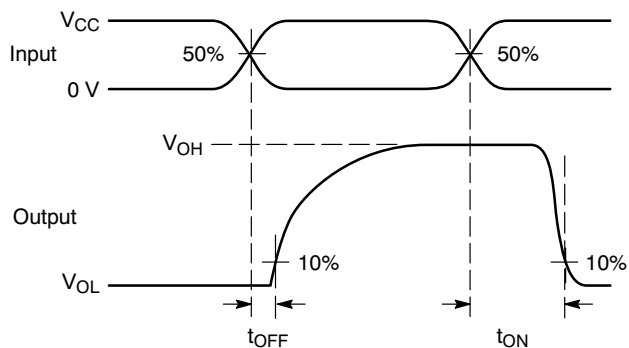
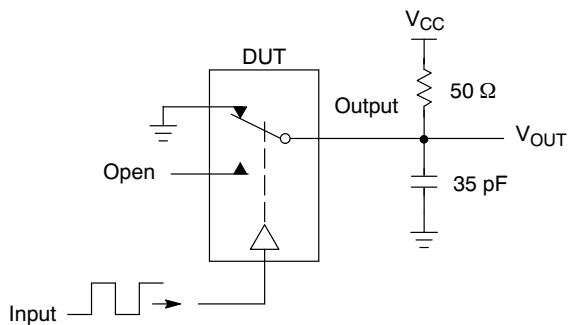
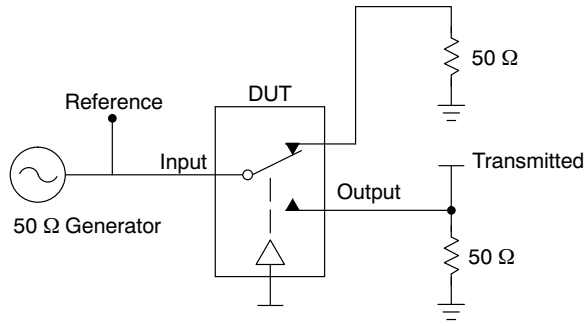


Figure 4. t_{ON}/t_{OFF}

NLAS5223B, NLAS5223BL



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

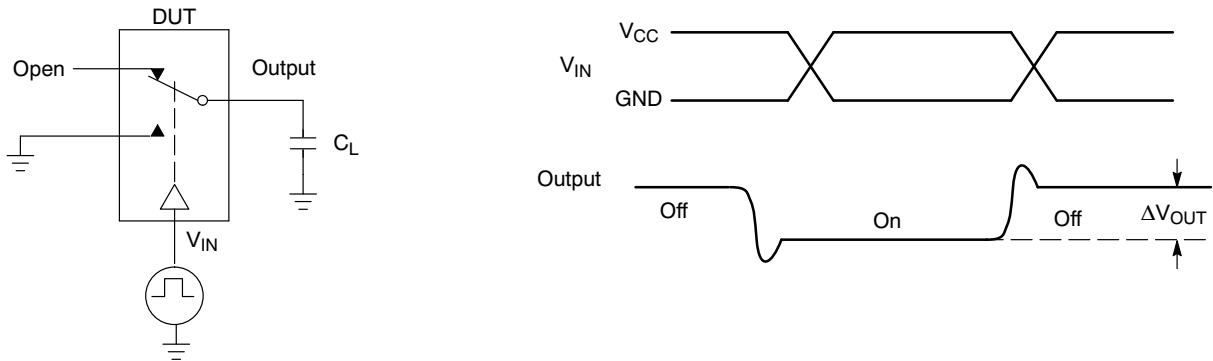


Figure 6. Charge Injection: (Q)

NLAS5223B, NLAS5223BL

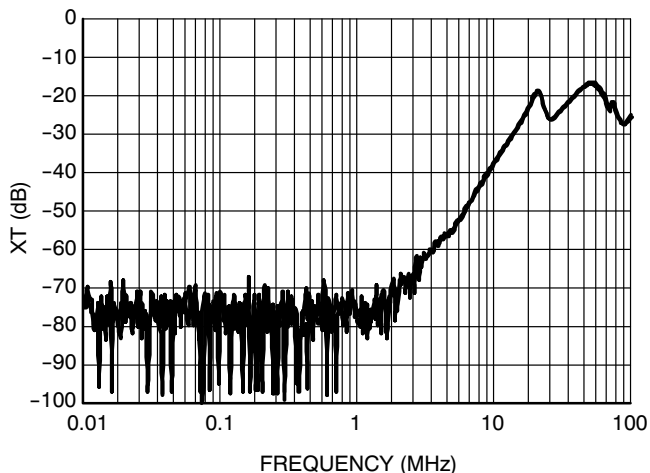


Figure 7. Cross Talk vs. Frequency
@ $V_{CC} = 4.3 \text{ V}$

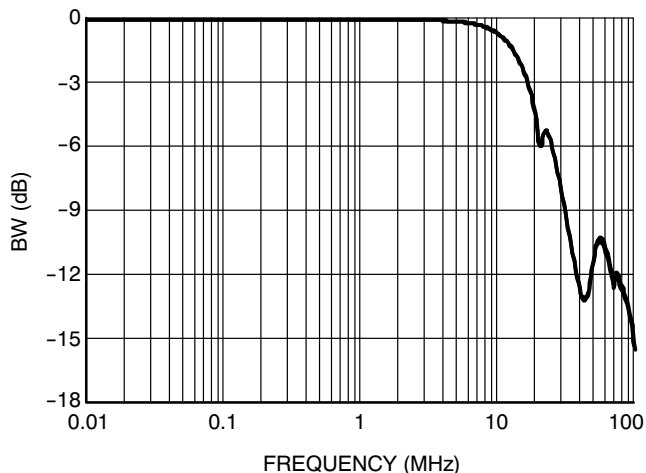


Figure 8. Bandwidth vs. Frequency

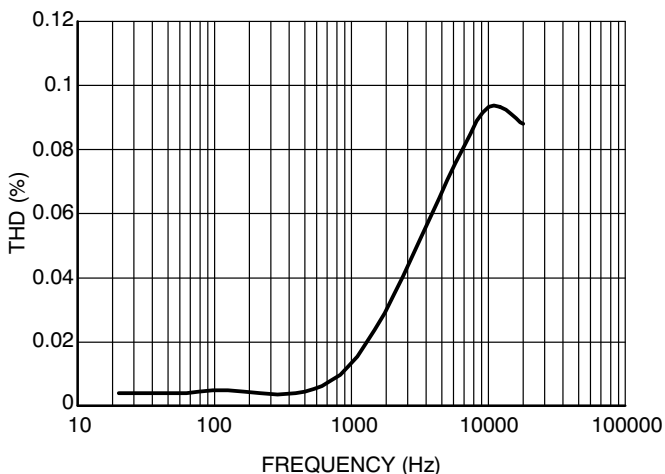


Figure 9. Total Harmonic Distortion

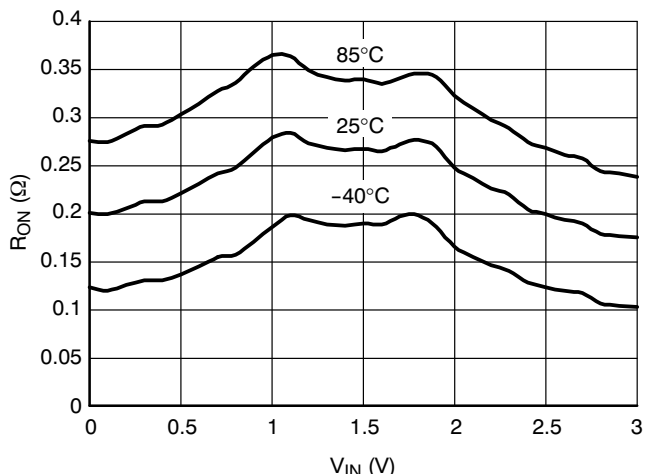


Figure 10. On-Resistance vs. Input Voltage
@ $V_{CC} = 3.0 \text{ V}$

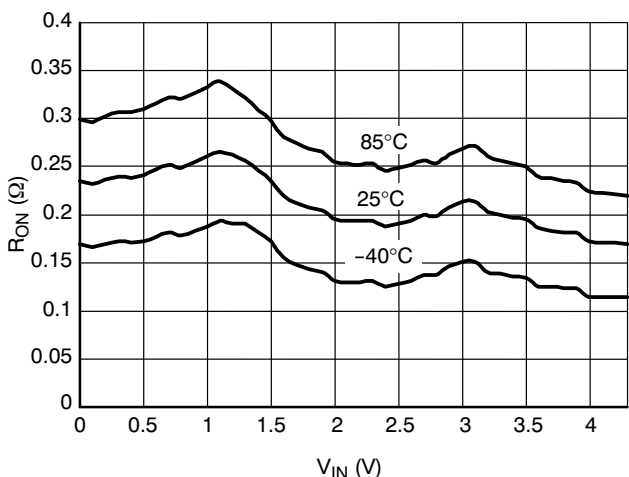


Figure 11. On-Resistance vs. Input Voltage
@ $V_{CC} = 4.3 \text{ V}$

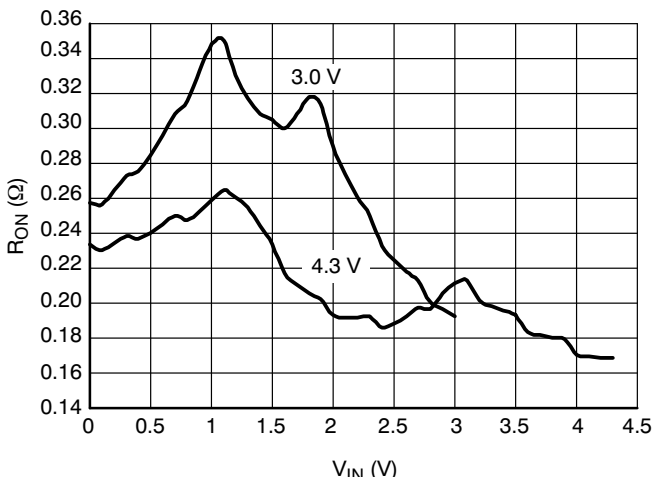


Figure 12. On-Resistance vs. Input Voltage

NLAS5223B, NLAS5223BL

ORDERING INFORMATION

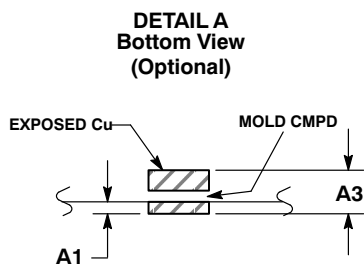
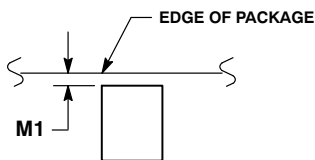
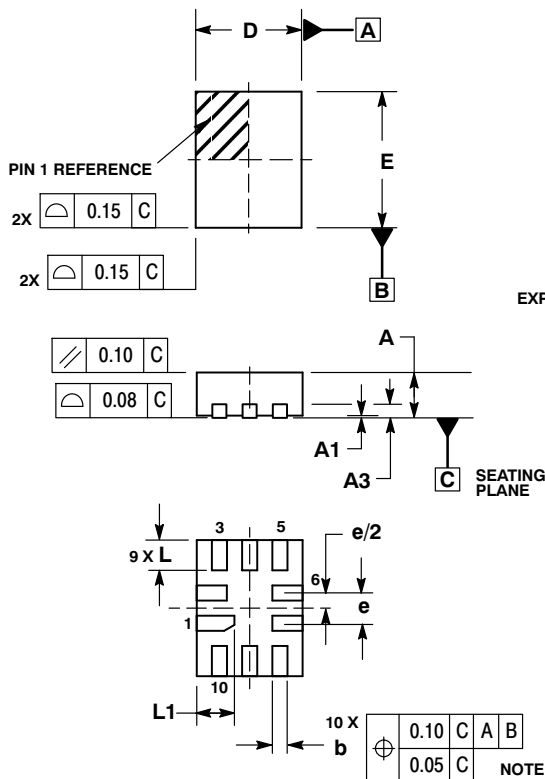
| Device | Package | Shipping [†] |
|-----------------|---------------------|-----------------------|
| NLAS5223BMNR2G | WQFN10 (Pb-Free) | 3000 / Tape & Reel |
| NLAS5223BLMNR2G | WQFN10 (Pb-Free) | 3000 / Tape & Reel |
| NLAS5223BMUR2G | UQFN10 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLAS5223B, NLAS5223BL

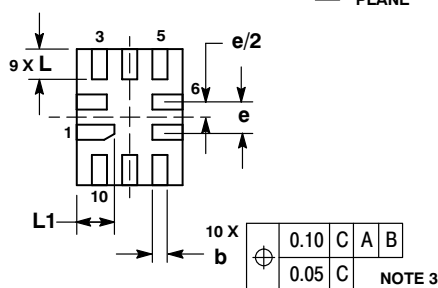
PACKAGE DIMENSIONS

WQFN10, 1.4x1.8, 0.4P
CASE 488AQ-01
ISSUE C

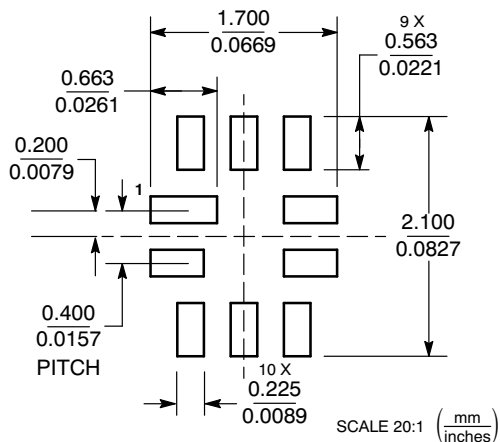


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

| MILLIMETERS | | |
|-------------|------|-------|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.050 |
| A3 | 0.20 | REF |
| b | 0.15 | 0.25 |
| d | 1.40 | BSC |
| E | 1.80 | BSC |
| e | 0.40 | BSC |
| L | 0.30 | 0.50 |
| L1 | 0.40 | 0.60 |
| M1 | 0.00 | 0.05 |



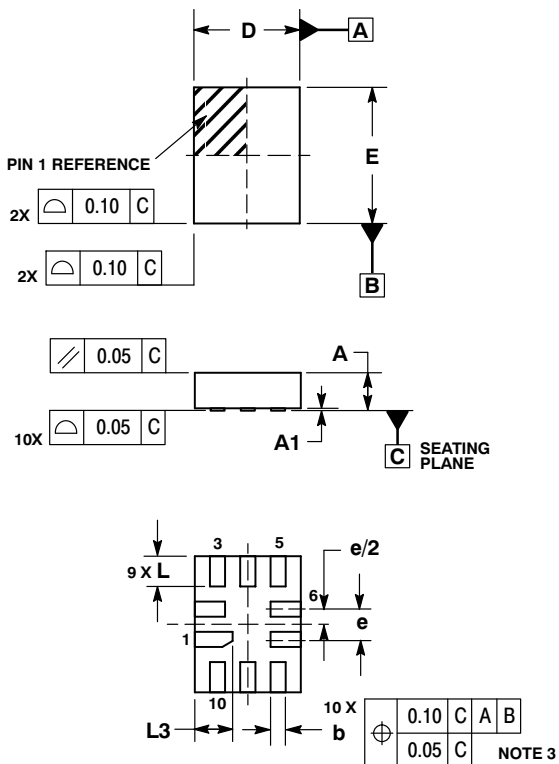
MOUNTING FOOTPRINT



NLAS5223B, NLAS5223BL

PACKAGE DIMENSIONS

UQFN10, 1.4x1.8, 0.4P
CASE 488AT-01
ISSUE O

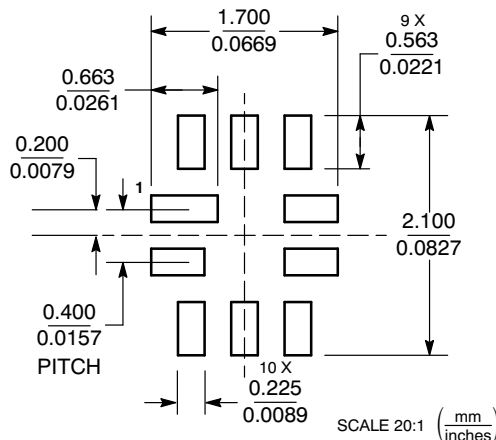


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.45 | 0.60 |
| A1 | 0.00 | 0.05 |
| b | 0.15 | 0.25 |
| D | 1.40 BSC | |
| E | 1.80 BSC | |
| e | 0.40 BSC | |
| L | 0.30 | 0.50 |
| L3 | 0.40 | 0.60 |

MOUNTING FOOTPRINT



ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative